EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	21	CMOS same LVT	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/21 15:27
S2	2	CMOS same LVT same (mixed hybrid)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/21 15:28
S3	2	CMOS same LVT same (mixed hybrid) and latch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/21 15:28
S4	9	CMOS and LVT and (mixed hybrid) and latch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 17:14
S5	5	CMOS and LVT and (mixed hybrid) and latch and power near10 reduc$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/21 15:29
S6	3	CMOS and LVT and (mixed hybrid) and latch and power near10 reduc$3 and scan$7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/21 15:31
S8	1	CMOS and LVT and (mixed hybrid) and latch and power near10 reduc$3 and scan$7 and RVT	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/21 15:33
S9	3	CMOS and LVT and (mixed hybrid) and latch and power near10 reduc$3 and scan$7 and leakage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/21 15:31

EAST Search History

S10	3	CMOS and LVT and (mixed hybrid) and latch and power near10 reduc$3 and scan$7 and threshold	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/02 10:42
S13	1052	mix$3 same threshold and (CMOS FET)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:45
S14	1	mix$3 near5 threshold same (CMOS FET) same (data clock) adj2 path	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:47
S15	1	mix$3 near5 threshold same (CMOS FET) and (data clock) adj2 path	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:47
S16	3	mix$3 near5 threshold same (CMOS FET) and (data clock) same path	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:48
S17	3	mix$3 near5 threshold same (CMOS FET) and (data clock) same path and section and critical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:48
S18	3	mix$3 with threshold same (CMOS FET) and (data clock) same path and section and critical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:48
S19	17	mix$3 with threshold and (CMOS FET) and (data clock) same path and section and critical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:49

EAST Search History

S20	29	mix$3 with threshold and (CMOS FET) and (data clock) and section and critical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:50
S21	34	(hybrid mix$3) with (threshold LVT) and (CMOS FET) and (data clock) and section and critical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:50
S22	13	(hybrid mix$3) with (threshold adj2 voltage LVT) and (CMOS FET) and (data clock) and section and critical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:51
S23	29	(hybrid mix$3) with (threshold adj2 voltage LVT) and (CMOS FET) and (data clock) and critical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:51
S24	134	(hybrid mix$3) with (threshold adj2 voltage LVT) and (CMOS FET) and (data clock)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 15:35
S25	42	(hybrid mix$3) with (threshold adj2 voltage LVT) and (CMOS FET) and (data clock) and (power near10 (reduc$3 minimiz$3 optimiz$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:52
S26	42	(hybrid mix$3) with (threshold adj2 voltage LVT) and (CMOS FET) and (data clock) and (power near10 (enhanc$3 reduc$3 minimiz$3 optimiz$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:53
S27	20	(hybrid mix$3) with (threshold adj2 voltage LVT) and (CMOS FET) and (data clock) and (power near10 (enhanc$3 reduc$3 minimiz$3 optimiz$3)) and (latch flip adj2 flop)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:55

EAST Search History

S28	6	(hybrid mix$3) with (threshold adj2 voltage LVT) and (CMOS FET) and (data clock) and (power near10 (enhanc$3 reduc$3 minimiz$3 optimiz$3)) and (latch flip adj2 flop) and dissipation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 10:56
S30	90	(LVT or low adj threshold adj voltage) and (mix$3 hybrid) and critical near6 (block circuit sub cell macro path)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 15:35
S31	1275354	(latch flip adj2 flop register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 15:16
S32	59	S30 and S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 15:16
S33	52	S30 and S31 and (clock clk sclk scan adj2 clock scan$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 15:32
S41	11319	(low high nominal) adj3 threshold adj1 voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 15:33
S42	51	S41 and S33	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 15:34
S43	3	S41 and S33 and output adj2 buffer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 15:34

EAST Search History

S44	45	(hybrid mix$3) with (threshold adj2 voltage LVT) and (CMOS FET) and (data clock) and (power with (reduc$3 enhanc$3 minimiz$3) dissipation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 16:38
S45	45	(hybrid mix$3 MVT) with (threshold adj2 voltage LVT) and (CMOS FET) and (data clock) and (power with (reduc$3 enhanc$3 minimiz$3) dissipation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 16:39
S46	45	(hybrid mix$3) with (threshold adj2 voltage LVT MVT) and (CMOS FET) and (data clock) and (power with (reduc$3 enhanc$3 minimiz$3) dissipation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 17:11
S47	507	(hybrid mix$3 multiple) same (threshold adj2 voltage LVT MVT) and (CMOS FET) and (data clock) and (power with (reduc$3 enhanc$3 minimiz$3) dissipation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 17:13
S48	503	(hybrid mix$3 multiple) same (threshold adj2 voltage LVT MVT) and (CMOS FET) and (data clock) and (power with (reduc$3 enhanc$3 minimiz$3) dissipation) and (nominal high regular)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 17:13
S49	18	(hybrid mix$3 multiple) same (threshold adj2 voltage LVT MVT) and (CMOS FET) and (data clock) and (power with (reduc$3 enhanc$3 minimiz$3) dissipation) and (nominal high regular) and 716/1-18.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 17:19
S50	11	(hybrid mix$3 multiple) same (threshold adj2 voltage LVT MVT) and (CMOS FET) and (data clock) and (power with (reduc$3 enhanc$3 minimiz$3) dissipation) and (nominal high regular) and (latch FF flip adj2 flop)and 716/1-18.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 17:19
S54	23	latch same mixed same threshold	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/22 20:00

EAST Search History

S55	5	CMOS and LVT and (mixed hybrid) and latch and scan$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 17:14
S56	13	CMOS and (low adj voltage adj threshold LVT) and (mixed hybrid dual multi) and (latch FF flip-flop flip adj2 flop) and scan$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 17:29
S57	22	CMOS and (low adj voltage adj threshold LVT) and (mixed hybrid dual multi) and (latch FF flip-flop flip adj2 flop) and (test$3 scan$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 17:34
S58	24	CMOS and (low adj voltage adj threshold LVT) and (mixed hybrid dual multi) and (latch FF flip-flop flip adj2 flop) and (test$3 scan$4 content)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 17:37
S59	30	CMOS and (low adj voltage adj threshold LVT) and (mixed hybrid dual multi) and (latch FF flip-flop flip adj2 flop memory adj cell) and (test$3 scan$4 content)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 18:00
S60	47	CMOS and ((low normal regular high) adj voltage adj threshold LVT RVT HVT) and (mixed hybrid dual multi) and (latch FF flip-flop flip adj2 flop memory adj cell) and (test$3 scan$4 content)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 18:02
S61	73	scan$4 and ((low normal regular high) adj voltage adj threshold LVT RVT HVT) and (mixed hybrid dual multi) and (latch FF flip-flop flip adj2 flop memory adj cell) and (test$3 content)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 18:14
S62	297	((low normal regular high) adj voltage adj threshold LVT RVT HVT) and (mixed hybrid dual multi) and (latch FF flip-flop flip adj2 flop memory adj cell) and (test$3 content)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 18:14

EAST Search History

S63	6885	scan$3 adj2 (latch register FF flip-flop flip adj2 flop)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 18:03
S64	6	S62 and S63	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 18:03
S65	452	((low normal regular high) adj voltage adj threshold LVT RVT HVT) and (mixed hybrid dual multi) and (latch FF flip-flop flip adj2 flop memory adj cell register) and (test$3 content leakage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 18:15
S66	99	((low normal regular high) adj voltage adj threshold LVT RVT HVT) and (mixed hybrid dual multi) same (latch FF flip-flop flip adj2 flop memory adj cell register) and (test$3 content leakage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 18:37
S67	17	((low normal regular high) adj voltage adj threshold LVT RVT HVT) and (mixed hybrid dual multi) and (latch FF flip-flop flip adj2 flop memory adj cell register) and critical adj path	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 18:38
S68	1192	716/2.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/02 10:42
S69	117	CMOS and (LVT low adj threshold adj voltage) and (mixed hybrid dual multi) and (register FF flip adj2 flop latch) and (test$3 scan$7) and leakage adj current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/02 10:45
S70	10	critical adj path and LVT	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/03 15:25

EAST Search History

S71	86	critical adj path and (LVT low adj threshold) and latch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/03 15:45
S73	3	critical adj path and (LVT low adj threshold) with output adj2 buffer and (register flip adj2 flop latch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/03 15:55
S74	21	critical adj path and (LVT low adj threshold) and output and buffer and (register flip adj2 flop latch) adj2 circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/03 16:04
S75	21	critical adj path and (LVT low adj threshold) and buffer and (register flip adj2 flop latch) adj2 circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/03 16:04